Docket No.: 03-0805 PATENT

UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Sean C. Erickson, et al.	:	By the Examiner:
Serial No.:	:	
Filed: July 25, 2003	:	Group Art Unit:

Title: LOW GATE RESISTANCE LAYOUT PROCEDURE FOR RF TRANSISTOR DEVICES

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATION UNDER 37 C.F.R. §1.10

I hereby certify that this Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date, July 25, 2003 in an envelope as "Express Mail Post Office to Addressee", Mailing Label No. EV 338 284 150 US addressed to: MS Patent Application, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

ReNea D. Berggren DATED: July 25, 2003

Dear Sir:

INFORMATION DISCLOSURE STATEMENT

Applicant submits herewith patents, publications or other information of which he is aware, which he believes may be material to the patentability of this application and in respect of which there may be a duty to disclose in accordance with 37 CFR 1.56.

While this Information Disclosure Statement may be "material" pursuant to 37 CFR 1.56, it is not intended to constitute an admission that any patent, publication or other information referred to herein is "prior art" for this invention unless specifically designated as such.

In accordance with 37 CFR 1.97(g) the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 CFR 1.56(a) exists.

The attached form, PTO-1449, provides a listing of patents, publications, or other information as required by 37 CFR 1.98(a)(1).

A copy of each of these items on PTO-1449 is supplied herewith.

Please direct all correspondence and telephone calls to:

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DATED: July 25, 2003.

Respectfully submitted,
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In Place of FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

Serial No.:
Applicant: Sean C. Erickson, et al.
Filing Date: July 25, 2003
Group:
Atty. Docket No.: 03-0805

Reference Designation

U.S. PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
AAA	6,544,829	04/08/03	Gopinath et al.	438	232	09/20/02
ABA	6,269,472	07/31/01	Garza et al.	716	21	12/12/97
ACA	5,705,301	01/06/98	Garza et al.	430	5	02/27/96
ADA						
AEA						
AFA						
AGA						
AHA						
AIA						
AJA						

FOREIGN PATENT DOCUMENTS

Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes No
AKA						
ALA						
AMA						
ANA						
AOA						

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

Examiner Initial

____ APA Weste, Neil et al.; Principles of CMOS VLSI Design; Addison-Wesley Pub. Co.; October, 1994; 113-116, 132-133

____ AQA Sze; VLSI Technology; McGraw-Hill; 1988; pgs. 416-417

____ ARA

Examiner: Date Considered:

EXAMINER: Initial if reference considered, whether nor not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.